IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re: Attorney Docket No. Balay 2-1

In re application of: Francois Balay et al.

Serial No.:	09/966,095	Group Art Unit:	2111
Filed:	10/01/01	Examiner:	Khanh Dang
Matter No.:	992.1508	Phone No.:	571-272-3626

For: PCI/LVDS Half Bridge

APPELLANTS' CORRECTED SUMMARY OF CLAIMED SUBJECT MATTER UNDER 37 CFR 41.37(c)(1)(v)

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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ATTENTION: Board of Patent Appeals and Interferences

In response to the Notifications of Non-Compliant Appeal Brief dated 6/10/09 and 6/19/09, the Applicants submit this corrected Summary of the Claimed Subject Matter in support of the appeal. This corrected Summary replaces the Summary of the Claimed Subject Matter previously presented on pages 5-6 of the Corrected Appeal Brief filed February 27, 2007.

(5) **SUMMARY OF CLAIMED SUBJECT MATTER (37 CFR 41.37(c)(1)(v))**

Compact PCI (Peripheral Component Interconnect) has become a standard implementation for many telecommunications systems. Compact PCI provides a well-standardized backplane structure. With PCI, different line cards or blades of a system are connected with a PCI bus structure. As with any bus structure, the number of line cards that can be connected on a single PCI bus is limited. Typically five line cards are supported on a 33MHz PCI bus structure. For larger systems, multiple independent PCI segments have to be implemented, each supporting a limited number of elements.

Embodiments of the invention provide a system and method of overcoming the limitations associated with the number of line cards that can be connected to on a single bus through use of half bridge circuits connecting the bus segments. In particular, depending on the particular application, e.g., latency considerations, the data paths connecting the half-bridge circuits are scalable to rely on more or less signal lines as needed for a particular application.

Independent claim 1 recites a system (such as, but not limited to, the system comprising elements 4 to 6 shown in Fig. 1 and described on page 5, lines 7-15) for interconnecting two or more computer bus architectures (such as, but not limited to, elements 3 and 7 shown in Fig. 1). The system includes a first bus segment (such as, but not limited to, element 3) to transmit data information, a first half-bridge circuit (such as, but not limited to, element 4) to connect the first bus segment, a second bus segment (such as, but not limited to, element 7) to transmit data information, a second half-bridge circuit (such as, but not limited to, element 6) to connect the first half-bridge circuit and to transfer data information between the first bus segment and the second bus segment; and a plurality of data paths (such as, but not limited to, element 5) to connect the first half-bridge circuit and the second half bridge circuit. The operation of the embodiment shown in Fig. 1 is described on page 5, line 16, through page 6, line 2, and on page 6, lines 15-26, of the specification. Importantly, claim 1 requires that the plurality of data paths connecting the first half-bridge circuit and the second half-bridge circuit are **scalable to correspond to a bandwidth needed for a particular application.** The scalability of the plurality of data paths is described in the specification on page 6, lines 9-14, and on page 10, lines 6-10.

Independent claim 10 recites a method of interconnecting two or more computer bus architectures. An embodiment of the method is described, e.g., on page 5, line 7, through page 6, line 2, and on page 6, lines 15-26, of the specification, with reference to the system depicted in Fig. 1. A first half bridge circuit (such as, but not limited to, element 4) is connected to a first bus segment (such as, but not limited to, element 3). A second half bridge circuit (such as, but not limited to, element 6) is connected to a second bus segment (such as, but not limited to, element 7). The first bus segment is connected to the second bus segment through a plurality of data paths (such as, but not limited to, element 5) connecting the first half-bridge circuit and the second half-bridge circuit. Data information is transmitted from the first bus segment to the second bus segment over at least one of the plurality of data paths. Importantly, the plurality of data paths connecting the first half bridge circuit and the second half bridge circuit are **scalable to correspond to a bandwidth needed for a particular application.** The scalability of the plurality of data paths is described in the specification on page 6, lines 9-14, and on page 10, lines 6-10.

Independent claim 19 recites a system (such as, but not limited to, the system comprising elements 4 to 6 shown in Fig. 1 and described on page 5, lines 7-15) for interconnecting two or more computer bus architectures. The system comprises a first half bridge circuit means (corresponding to element 4) connected to a first bus segment means (corresponding to element 3). A second half bridge circuit means (corresponding to element 6) is connected to a second bus segment means (corresponding to element 7). A plurality of data paths means (corresponding to element 5) connect the first half bridge circuit means and the second half bridge circuit means. Information is passed between the first bus segment means and the second bus segment means over the first half bridge circuit means and the second half bridge circuit

means. The operation of the embodiment shown in Fig. 1 is described on page 5, line 16, through page 6, line 2, and on page 6, lines 15-26, of the specification. Importantly, the plurality of data paths means are **scalable to correspond to a bandwidth needed for a particular application.** The scalability of the plurality of data paths is described in the specification on page 6, lines 9-14, and on page 10, lines 6-10.

Respectfully submitted,

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